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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,865	01/18/2002	Mario Saggio	00-CT-320	5366

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/053,865	SAGGIO ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 24 and 40 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 25 and 40 recite an unclear limitation, "the resistivity of said semiconductor material layer is less than five Ohm-cm." Note that this range of the resistivity requires at least a voltage or a voltage range.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 22-34 and 36-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Silber et al. (DE 198 20 734), hereinafter Silber in view of Fujihira (US 6683347)

Regarding claim 22, Figure 6 of Silber shows a Schottky barrier diode formed through a method comprising:

forming a substrate region [3] of a first conductivity type [n+] underneath a semiconductor material layer [2] of the same conductivity type [n];

forming a metal layer [1]; and

forming at least two doped regions [5, 56] of a second conductive type [p] formed in said semiconductor material layer, each one of said doped regions being disposed under said metal layer and being separated from the other doped region and said substrate region by portions of said semiconductor layer.

Figure 6 of Silber shows a method which forms substantially the entire claimed structure except "wherein said doped regions are formed by successive implants to form a plurality of stacked bubbles." Fujihira discloses a diode wherein the said doped regions [p] are formed by successive implants to form a plurality of stacked bubbles.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Fujihara into the device of Silber in order to have the doped regions formed by successive implants to form a plurality of stacked bubbles to improve a breakdown voltage.

Regarding claim 23, Fujihira discloses a method further comprising thermally processing said plurality of stacked bubbles (col. 7, lines 35-38).

Regarding claim 24, the combined teachings of Silber and Fujihara fails to disclose implanting said doped regions at a dose between 1×10^{12} and 5×10^{13} per cm^2. However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have an intended dose for the doped region recited in pending claim, since it would have been

held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller,* 105 USPQ 233.

Regarding claim 25, insofar as understood, Silber discloses the resistivity of said semiconductor material layer is less than 5 ohm-cm^2 to sustain 450V (col.2, lines 50-57).

Regarding claim 26, Silber discloses said semiconductor material layer.[2] comprises a first resistivity value, and said doped regions [5, 56] each comprise a second resistivity value , wherein said second resistivity vaiue is higher than said first resistivity value through disclosing that the the doping concentration of doped region [$10^{15}/cm^3$] is higher than the one in the semiconductor layer [2x $10^{14}/cm^3$].

Regarding claim 27, Fig. 6 of Silber shows said substrate comprises a doping value [n+] higher than a doping value [n] of said semiconductor material layer.

Regarding claim 28, Fig. 6 of Silber shows said doped regions further comprise respective body regions [5].

Regarding claim 29, Fig. 6 of Silber shows said doped regions further comprise heavily doped body regions [5] having the same conductivity type [p] of said doped regions [56].

Regarding claim 30, Fig. 6 of Silber shows said semiconductor material layer comprises a resistivity value lower than five Ohm-cm for a breakdown voltage higher than 200V (col. 3, lines 38-51).

Regarding claim 31, Fig. 6 of Silber shows said doped regions [5, 56]comprise P-type doped regions.

Regarding claim 32, Fig. 6 of Silber shows in which said semiconductor material layer [2] comprises an N-type serniconductor material layer.

Regarding claims 33 and 34, Fig. 6 of Silber shows in said Schottky barrier diode is operational at a voltage of 500V/600V (col.3, lines 38-51).

Regarding claim 36, Silber discloses that at least one of the doped regions is in an active area of said Schottky barrier diode and at least one of the doped regions is in an edge area of said Schottky barrier diode (col. 7, lines 38-43).

Regarding claim 37, Fujihira discloses said doped regions are formed by successive implants into successive growths of said semiconductor material layer (col. 15, lines 23-28).

Regarding claim 38, Fujihira discloses a method further comprising thermally processing said plurality of stacked bubbles (col. 7, lines 35-38).

Regarding claim 39, the combined teachings of Silber and Fujihira fails to disclose implanting said doped regions at a dose between 1×10^{12} and 5×10^{13} per cm^2. However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have an intended dose for the doped region recited in pending claim, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller,* 105 USPQ 233.

Regarding claim 40, insofar as understood, Silber discloses the resistivity of said semiconductor material layer is less than 5 ohm-cm^2 to sustain 450V (col.2, lines 50-57).

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Silber and Fujihira as applied to claims 1 above, and further in view of Readdie et al. (US 5254869), hereinafter Readdie.

Regarding claim 35, the combined teachings of Silber and Fujihira fails to show a silicide layer over the semiconductor material layer. Fig. 4 of Readdie shows a Schottky diode wherein a silicide layer (401a) formed over the semiconductor layer (101) and below the metal layer (105a). It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Readdie into the device of Silber and Fujihira in order to have a silicide layer over the semiconductor layer and below the metal layer so as to reduce the diffusion of the metal into the semiconductor (Abstract).

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

Steven Loke
Primary Examiner